1.8V - 6.5V、750mA、60nA I_Q 降压转换器

特性

- 60nA 工作静态电流
- 100% 占空比模式下，I_Q 为 120nA
- 输入电压范围 V_{IN}：1.8V 至 6.5V
- 高达 750mA 的输出电流
- 射频友好型 DCS-Control™
- 1μA I_{OUT}（3.6V_{IN} 至 1.8V_{OUT}）时的效率为 80%
- 通过 VSET 引脚提供 16 种可选输出电压
- 自动转换 PFM/PWM 或强制 PWM 模式
- 可选的强制 PWM 和 STOP 模式
- 输出放电功能
- 25nA 关断电流
- SON-8P、WCSP-6P

概述

SR62840 是一款高效降压转换器，具有典型值为 60nA 的超低工作静态电流。此器件具有特殊电路，可在 100% 模式下实现仅 120nA 的 I_Q，因此可在放电末期进一步延长电池寿命。

此器件采用 DCS-Control 技术，可以为无线电提供干净的电源，工作时具有 1.8MHz 的典型开关频率。在省电模式下，此器件可将轻负载效率向下扩展至 1μA 负载电流及以下。

可以将一个电阻器连接到 VSET 引脚以选择 16 种预定义的输出电压，因此这款器件可以灵活地用于各种 应用 并最大限度地减少了外部组件的数量。

该器件的 STOP 引脚可立即消除所有的开关噪声，从而在测试和测量系统中执行无噪声测量。

SR62840 提供了高达 750mA 的输出电流。此器件的输入电压为 1.8V 至 6.5V，支持多种电源，例如 2 节至 4 节碱性电池或 1 节至 2 节锂二氧化锰 (Li-MnO_2) 或 1 节锂离子/锂亚硫酰氯 (Li-$SOCl_2$) 电池。

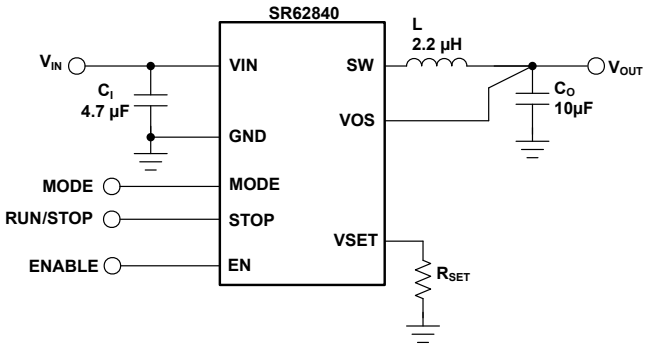
器件信息

器件型号	封装	封装尺寸（标称值）
SR62840DLC	SON-8P	1.5mm x 2mm
SR62840YBG	WCSP-6P	0.97mm x 1.47mm

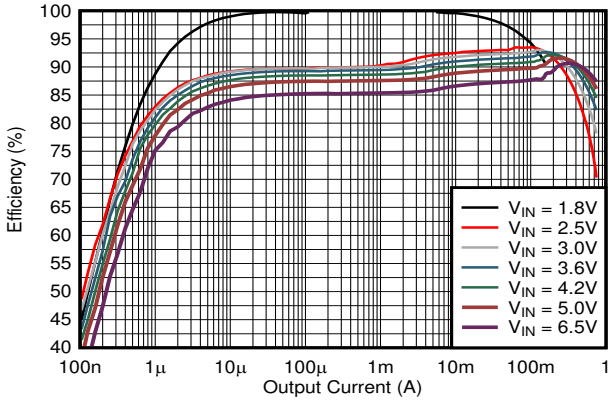
应用领域

- 智能仪表、智能恒温器
- 资产跟踪设备
- 可穿戴电子产品
- 医疗传感器贴片和患者监护仪
- 工业物联网（智能传感器）/窄带物联网
- 测试和测量
- ATEX/本质安全

典型应用电路



效率与负载电流间的关系 (V_{OUT} = 1.8V)

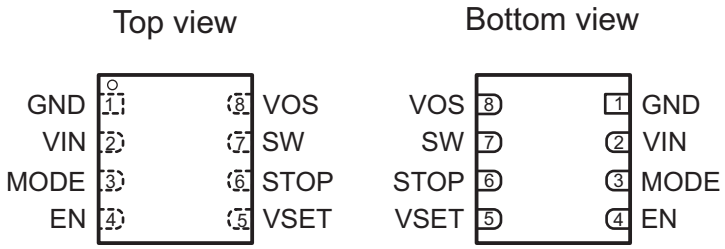


Device Comparison Table

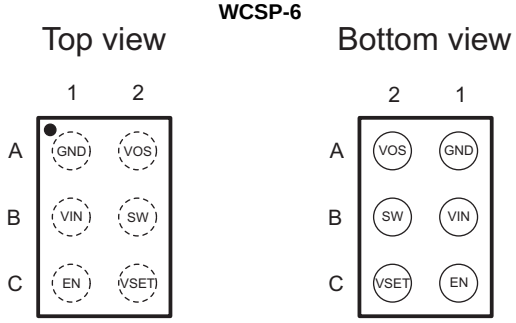
ORDERABLE PART NUMBER	OUTPUT VOLTAGE	OUTPUT CURRENT	OUTPUT DISCHARGE	MODE PIN	STOP PIN	PACKAGE	PACKAGE MARKING
SR62840DLC	1.8 V to 3.3 V in 100-mV steps	750 mA	yes	yes	yes	SON-8	E5
SR62840YBG				no	no	WCSP-6	62840

Pin Configuration and Functions /引脚定义与功能描述

SON-8



WCSP-6



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DLC (SON-8)	DGR (HVSSOP-8)	YBG (WCSP-6)		
VIN	2	6	B1	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A 4.7-µF ceramic capacitor is required.
SW	7	2	B2	PWR	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
GND	1	8	A1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitors.
VSET	5	4	C2	IN	Connecting a resistor to GND sets the output voltage when the converter is enabled. For the SR62840, connect this pin to GND.
VOS	8	1	A2	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. When the converter is disabled, this pin discharges V_{OUT} by an internal MOSFET. Connect this pin directly to the output capacitor with a short trace.
EN	4	5	C1	IN	Enable pin. A high level enables the device and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up and the output voltage is regulated. The pulldown resistor is activated again, once a low level has been detected.
STOP	6	n/a	n/a	IN	STOP Switching pin. When this pin is logic high, the converter stops switching in order to provide a quiet supply rail. The output is powered from the charge available in the output capacitor. When this pin is logic low, the device immediately resumes operation. The pin features an internal pulldown resistor, which is disabled once a high level is detected at the input. The pulldown resistor is activated again, once a low level has been detected.
MODE	3	3	n/a	IN	MODE pin. A low level enables Power-Save Mode operation with an automatic transition between PFM and PWM modes. A high level forces the converter to operated in PWM mode. This pin can be toggled during operation. It must be terminated.
NC	n/a	7	n/a		This pin is not connected internally. Do not connect this pin.
EP	n/a	9	n/a	PWR	Exposed thermal pad . The PowerPAD must be connected to GND.

Specifications/技术参数

Absolute Maximum Ratings / 极限参数

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	7	V
	SW (DC)	–0.3	V_{IN} + 0.3	V
	SW (AC), less than 10ns	–2.0	8.5	V
	EN, MODE, STOP	–0.3	6.5	V
	VSET	–0.3	V_{IN} + 0.3 < 3.6	V
	VOS	–0.3	3.7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) While switching.

ESD Ratings / 静电放电参数

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions / 推荐操作条件

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}	1.8		6.5	V
L	Effective inductance	1.51	2.2	2.9	µH
C_{OUT}	Effective output capacitance	3	10	40	µF
C_{IN}	Effective input capacitance	1	4.7		µF
C_{VSET}	External parasitic capacitance at VSET pin			100	pF
R_{SET}	Nominal resistance range for external voltage selection resistor (E96 resistor series)	0.909		267	kΩ
	External voltage selection resistor tolerance			1%	
	External voltage selection resistor temperature coefficient			±200	ppm/°C
T_J	Operating junction temperature range	-40		125	°C

Thermal Information / 热性能信息

THERMAL METRIC(1)		8 Pins DLC Package	6 Pins YBG Package	8 Pins DGR Package	DGR EVM	UNIT
		JEDEC PCB 51-7		JEDEC PCB 51-5	SR62840-2EVM123	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.6	133.4	54.4	46.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.7	0.4	58.1	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.9	39.4	25.9	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	0.1	1.2	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.5	39.4	25.9	17.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	11.7	N/A	°C/W

Electrical Characteristics / 电气特性

V_{IN} = 3.6 V, T_J = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at T_J = 25°C (unless otherwise noted)

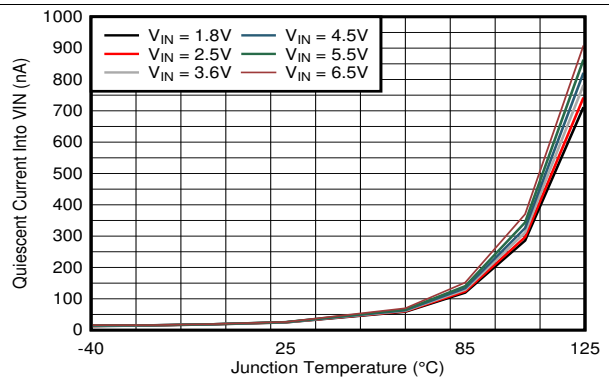
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q\_NO\_LOAD}$	No load operating input current	EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.8V device switching		60		nA
$I_{Q\_NO\_LOAD}$	No load operating input current	EN = $V_{IN,}$ I_{OUT} = 0μA, V_{OUT} = 1.2V device switching		80		nA
$I_{Q\_NO\_LOAD}$	No load operating input current (PWM Mode)	EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.8V, MODE = V_{IN} device switching		3		mA
I_{Q_VIN}	Operating quiescent current into pin VIN	EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = 25°C (DLC package option)		36	100	nA
I_{Q_VOS}	Operating quiescent current into pin VOS	EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = 25°C (DLC package option)		56	120	nA
I_{Q_VIN}	Operating quiescent current into pin VIN	EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = -40°C to 85°C		36	360	nA
I_{Q_VOS}	Operating quiescent current into pin VOS	EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V device not switching, T_J = -40°C to 85°C		56	170	nA
I_{Q_VOS}	Operating quiescent current into VOS pin	EN = V_{IN}, V_{OUT} = 3.3V device not switching		70		nA
		EN = V_{IN}, V_{OUT} < 1.5 V device not switching		5		nA
		EN, STOP = V_{IN}, 3V < V_{OUT} < 3.3V T_J = -40°C to 85°C		5	100	nA
$I_{Q\_100\%\_MODE}$	Operating quiescent current 100% Mode	V_{IN} = V_{OUT} = 3.3V, T_J = -40°C to 85°C		120		nA
$I_{Q\_VIN\_STOP}$	Operating quiescent current into pin VIN	STOP = High, V_{OUT} = 1.8V, T_J = -40°C to 85°C		70	175	μA
I_{SD}	Shutdown current	EN = GND, shutdown current into V_{IN} VSET = GND, T_J = -40°C to 85°C		25	300	nA
V_{TH_UVLO+}	Undervoltage lockout threshold	Rising V_{IN}		1.72	1.8	V
$V_{TH\_UVLO–}$		Falling V_{IN}		1.45	1.75	V
EN, MODE, STOP INPUTS						
V_{IH_TH}	High level input voltage		1.1			V
V_{IL_TH}	Low level input voltage				0.4	V
I_{IN}	Input bias current	MODE input, T_J = -40°C to 85°C		1	25	nA
R_{PD}	Internal pull-down resistance	EN, STOP inputs	200	450		kΩ

Electrical Characteristics (continued) / 电气特性(继续)

V_{IN} = 3.6 V, T_J = –40°C to 125°C, STOP = GND, MODE = GND, typical values are at T_J = 25°C (unless otherwise noted)

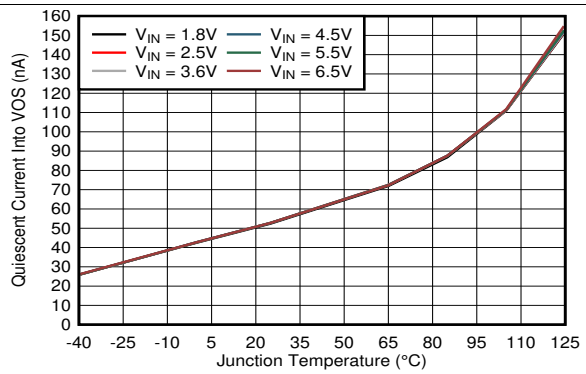
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCHES						
$R_{DS(ON)}$	High-side MOSFET on-resistance (DLC, YBG package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		430	600	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		340	465	
	Low-side MOSFET on-resistance (DLC, YBG package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		170	240	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		135	180	
	High-side MOSFET on-resistance (DGR package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		460	630	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		370	495	
	Low-side MOSFET on-resistance (DGR package)	V_{IN} = 3.6V, I = 200mA, T_J = -40°C to 85°C		200	270	mΩ
		V_{IN} = 5V, I = 200mA, T_J = -40°C to 85°C		165	210	
I_{LIMF_SS}	Soft-start switch current limit		0.15	0.225	0.3	A
I_{LIMF}	High-side MOSFET switch current limit(1)		1.0	1.2	1.4	A
	Low-side MOSFET switch current limit			1.0		A
I_{LIMN}	Negative current limit			533		mA
$t_{I\_LIM\_DELAY}$	Current limit propagation delay			50		ns
I_{LKG_SW}	Leakage current into SW pin	V_{SW} = 1.8V, T_J = -40°C to 85°C		10		nA
OUTPUT VOLTAGE DISCHARGE						
$I_{DISCHARGE\_VOS}$	Output discharge current	EN = GND, sink current into VOS pin, over VIN range V_{OUT} = 1.8V, T_J = -40°C to 85°C	16	35	44	mA
THERMAL PROTECTION						
T_{SD}	Thermal shutdown temperature	Rising junction temperature, PWM Mode		160		°C
	Thermal shutdown hysteresis			5		°C
OUTPUT						
V_{OUT}	Output voltage accuracy	PWM Mode, I_{OUT} = 0 mA, V_{OUT} >= 1.8 V	-1.5	0	1.5	%
		PWM Mode, I_{OUT} = 0 mA, V_{OUT} <= 1.55 V	-2	0	2	%
V_{OUT}	DC output voltage load regulation	PWM Mode		0		%/mA
	DC output voltage line regulation	PWM Mode V_{OUT} = 1.8V, I_{OUT} = 200 mA, over VIN range		0		%/V
f_{SW}	Switching frequency	V_{IN} = 3.6V, V_{OUT} = 1.8V, MODE = V_{IN} I_{OUT} = 0mA		1.8		MHz
$t_{STARTUP\_DELAY}$	Regulator start up delay time	V_{IN} = 3.6V, from EN = low to high until device starts switching			200	µs
$t_{STARTUP\_DELAY}$	Regulator start up delay time	EN ramps with VIN, VIN 0 to 3.6V (< 100us), until device starts switching		10		ms
t_{SS}	Soft-start time	I_{OUT} = 0mA		120		µs
t_{SS_ILIMF}	Reduced current limit soft-start timeout			700	1200	µs

Typical Characteristics / 典型特性



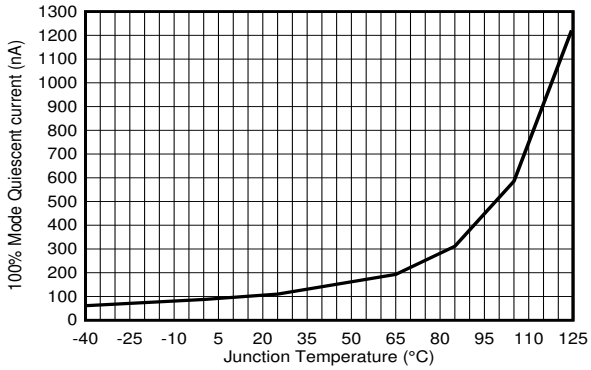
EN = VIN VOUT = 1.55 V Device Not Switching

1. Quiescent Current into VIN (I_{Q_VIN})



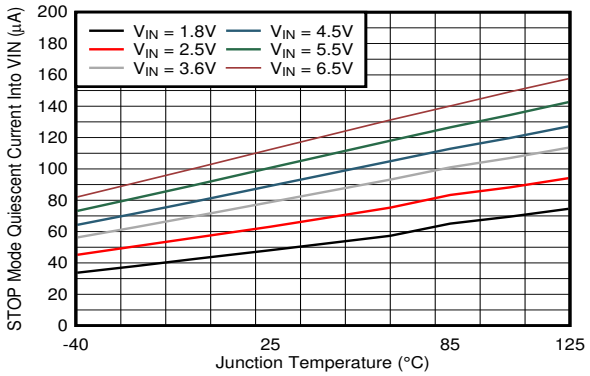
EN = VIN VOUT = 1.55 V Device Not Switching

2. Quiescent Current into VOS (I_{Q_VOS})



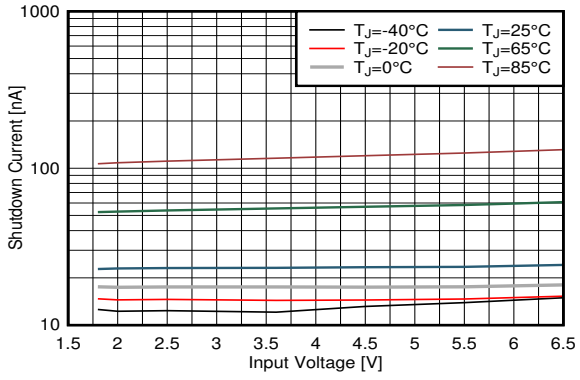
EN = VIN VIN = VOUT = 3.3 V Device Not Switching

3. 100% Mode Quiescent Current ($I_{Q\_100\%\_MODE}$)



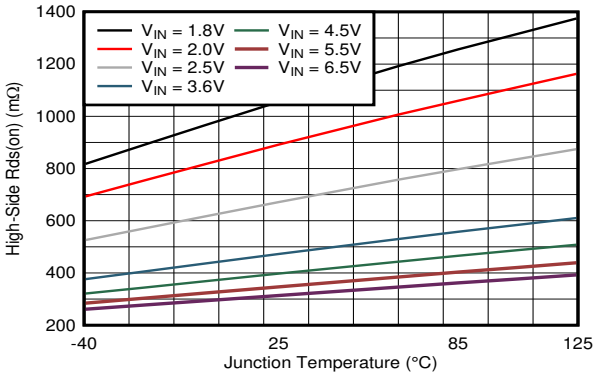
EN = VIN VOUT = 1.8 V Device Not Switching

4. STOP Mode Quiescent Current into VIN ($I_{Q\_VIN\_STOP}$)



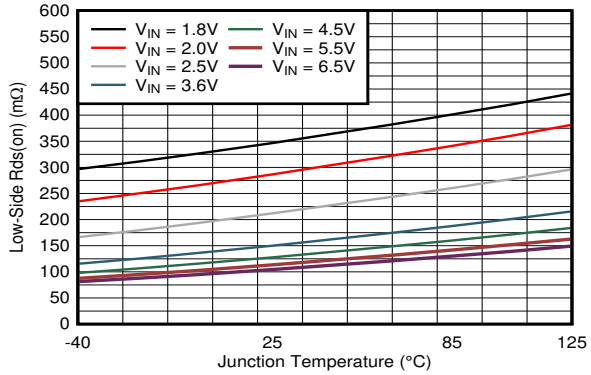
EN = GND

5. Shutdown Current (I_{SD})

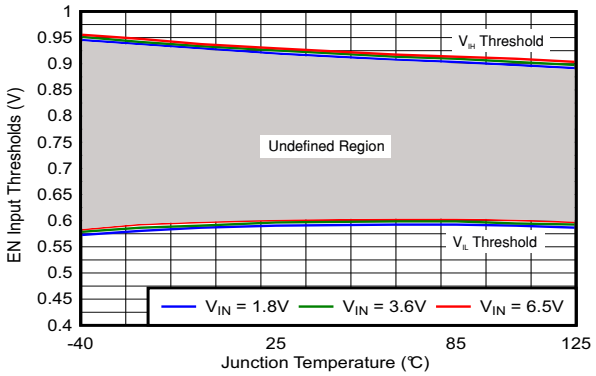


6. High-Side R_{DSON} versus Temperature (DLC, YBG packages)

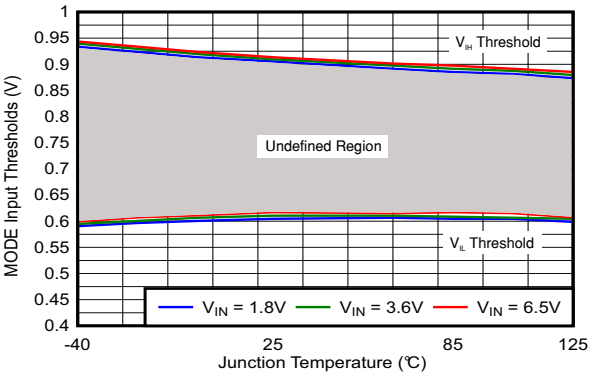
Typical Characteristics (Continue) / 典型特性(继续)



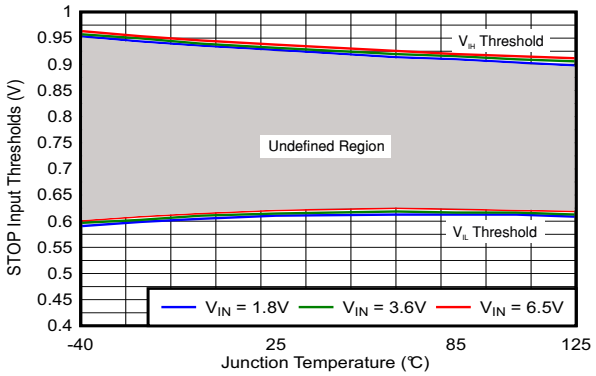
7. Low-Side R_{DSON} versus Temperature (DLC, YBG packages)



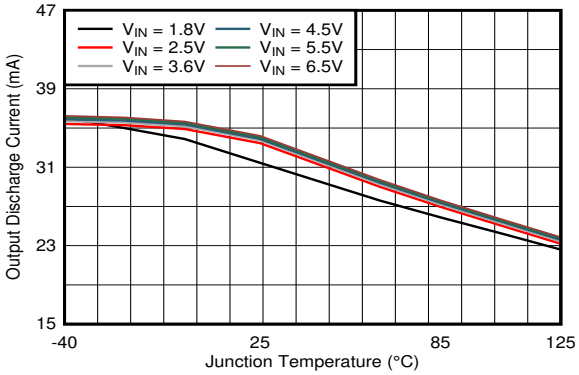
8. EN Input Thresholds versus Temperature



9. MODE Input Thresholds versus Temperature



10. STOP Input Thresholds versus Temperature



EN = GND VOUT = 1.8 V

11. Output Discharge Current versus Temperature