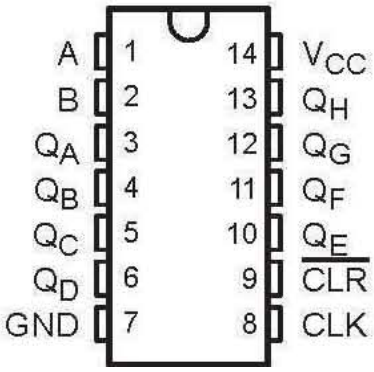
**Features**

- Wide Operating Voltage Range of 2 V to 6V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max $I_{CC}$
- Typical $t_{pd}$ =20 ns
- ±4-mA Output Drive at 5V
- Low Input Current of 1μA Max
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear

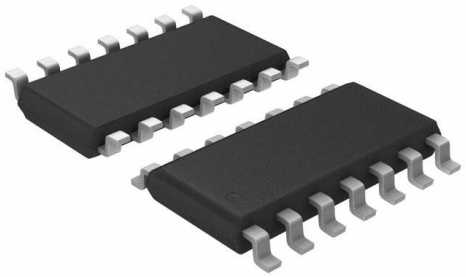
**Description/ordering information**

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) input permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

SR74HC164D
(TOP VIEW)




SR74HC164D
(3D VIEW)



**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PARTNUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| -40℃ to 85℃ | SOIC - D | Reel of 2500 | SR74HC164D | SR74HC164 |

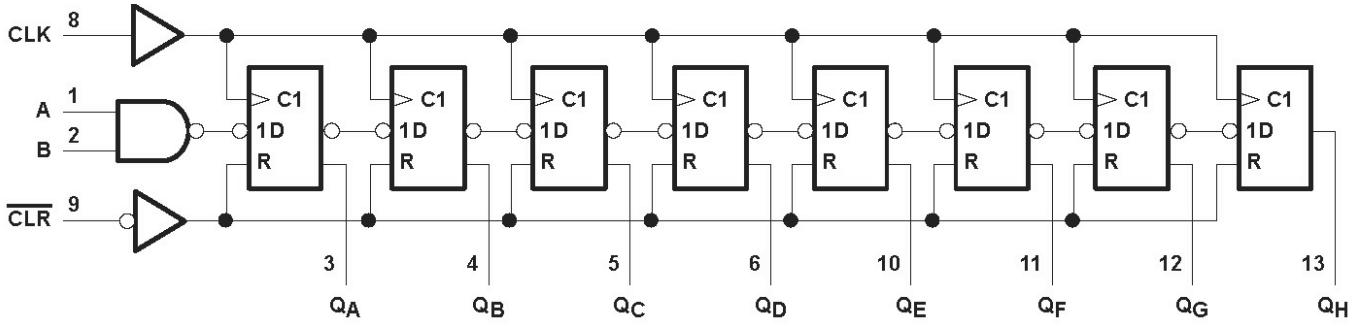
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | A | B | $Q_A$ | $Q_B$ … $Q_H$ | |
| L | X | X | X | L | L | L |
| H | L | X | X | $Q_{AO}$ | $Q_{BO}$ | $Q_{HO}$ |
| H | ↑ | H | H | H | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | $Q_{Gn}$ |

$Q_{A0}$, $Q_{B0}$,$Q_{H0}$ = the level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established

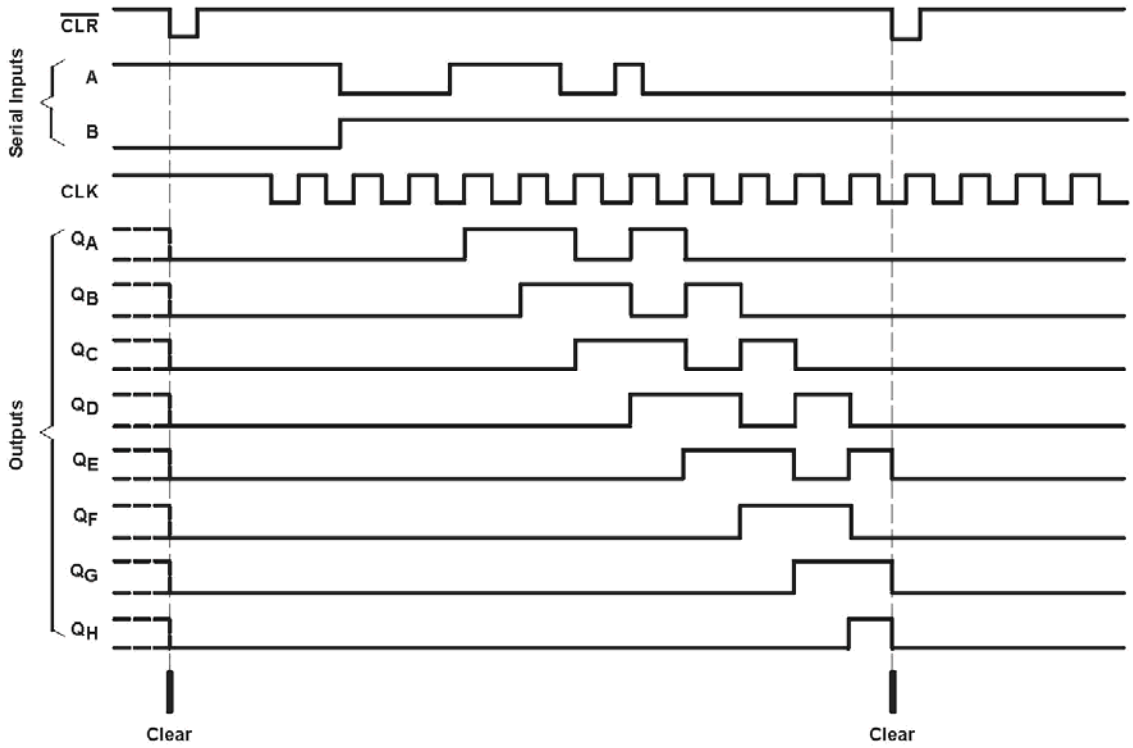
$Q_{An}$, $Q_{Gn}$ = the level of $Q_A$ or $Q_G$ before the most recent ↑ transition of CLK: indicates a 1-bit shift

**logic diagram (positive logic)**




Pin numbers shown are for the D packages.

**Typical clear, shift, and clear sequence**




**absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †**

Supply voltage range, $V_{CC}$……-0.5 V to 7 V
Input clamp current, $I_{IK}$($V_I$ < 0 or $V_I$ >$V_{CC}$ ) (see Note 1)……±20mA
Output clamp current, $I_{oK}$($V_o$ < 0 or $V_o$ >$V_{CC}$ ) (see Note 1)…… ±20mA
Continuous output current, $I_o$ ($V_o$ = 0 to $V_{CC}$ ) ……±25mA
Continuous current through $V_{CC}$ or GND……±50mA
Package thermal impedance,$\theta_{JA}$ (see Note 2): D package……86 ℃/W
Storage temperature range, $T_{stg}$ ……-65℃ to 150℃

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7

**Recommended operating conditions (see Note 3)**

| | | | | SR74HC164D | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$=2V | | 1.5 | | | V |
| | | $V_{CC}$=4.5V | | 3.15 | | | |
| | | $V_{CC}$=6V | | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$=2V | | | | 0.5 | V |
| | | $V_{CC}$=4.5V | | | | 1.35 | |
| | | $V_{CC}$=6V | | | | 1.8 | |
| $V_I$ | Input voltage | | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | | 0 | | $V_{CC}$ | V |
| △t /△v† | Input transition rise/fall time | $V_{CC}$=2V | | | | 1000 | ns |
| | | $V_{CC}$=4.5V | | | | 500 | |
| | | $V_{CC}$=6V | | | | 400 | |
| $T_A$ | Operating free-air temperature | | | -40 | | 85 | ℃ |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report. Implications of Slow or Floating CMOS Inputs, literature number SCBAOO4.

† If this device is used in the threshold region (from $V_{IL}$ max = 0.5V to $V_{IH}$ min =1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t$ =1000ns and $V_{CC}$ = 2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

**Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | | VCC | $T_A$ =25℃ | | | | SR74HC164D | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | MIN | MAX | |
| $V_{OH}$ | $V_I$= $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 μA | 2V | 1.9 | 1.998 | | | 1.9 | | V |
| | | | 4.5V | 4.4 | 4.499 | | | 4.4 | | |
| | | | 6V | 5.9 | 5.999 | | | 5.9 | | |
| | | $I_{OH}$ = -4mA | 4.5V | 3.98 | 4.3 | | | 3.84 | | |
| | | $I_{OH}$ = -5.2mA | 6V | 5.48 | 5.8 | | | 5.34 | | |
| $V_{OL}$ | $V_I$= $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2V | | 0.002 | 0.1 | | | 0.1 | V |
| | | | 4.5V | | 0.001 | 0.1 | | | 0.1 | |
| | | | 6V | | 0.001 | 0.1 | | | 0.1 | |
| | | $I_{OL}$ = 4mA | 4.5V | | 0.17 | 0.26 | | | 0.33 | |
| | | $I_{OH}$ = 5.2mA | 6V | | 0.15 | 0.26 | | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 6V | | ±0.1 | ±100 | | | ±1000 | nA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, | $I_O$ =0 | 6V | | | 8 | | | 80 | μA |
| $C_i$ | | | 2V to 6V | | 3 | 10 | | | 10 | pF |

**Timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

| | | $V_{CC}$ | $T_A$ =25℃ | | | SR74HC164D | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | | MIN | MAX | |
| $f_{clock}$ Clock frequency | | 2V | | 6 | | | 5 | MHz |
| | | 4.5V | | 31 | | | 25 | |
| | | 6V | | 36 | | | 28 | |
| $t_W$ Pulse duration | $\overline{CLR}$ low | 2V | 100 | | | 125 | | ns |
| | | 4.5V | 20 | | | 25 | | |
| | | 6V | 17 | | | 21 | | |
| | CLK high or low | 2V | 80 | | | 100 | | |
| | | 4.5V | 16 | | | 20 | | |
| | | 6V | 14 | | | 18 | | |
| $t_{su}$ Setup time before CLK↑ | Data | 2V | 100 | | | 125 | | ns |
| | | 4.5V | 20 | | | 25 | | |
| | | 6V | 17 | | | 21 | | |
| | $\overline{CLR}$ inactive | 2V | 100 | | | 125 | | |
| | | 4.5V | 20 | | | 25 | | |
| | | 6V | 17 | | | 21 | | |
| $t_h$ Hold time, data after CLK↑ | | 2V | 5 | | | 5 | | ns |
| | | 4.5V | 5 | | | 5 | | |
| | | 6V | 5 | | | 5 | | |

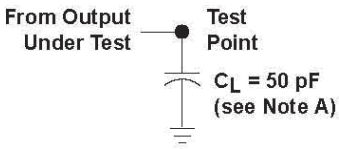
**Switching characteristics over recommended operating free-air temperature range, CL = 50pF (unless otherwise noted) (see Figure1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ =25℃ | | | | SR74HC164D | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | MIN | MAX | |
| $f_{max}$ | | | 2V | 6 | 10 | | | 5 | | MHz |
| | | | 4.5V | 31 | 54 | | | 25 | | |
| | | | 6V | 36 | 62 | | | 28 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 2V | | 140 | 205 | | | 255 | Ns |
| | | | 4.5V | | 28 | 41 | | | 51 | |
| | | | 6V | | 24 | 35 | | | 46 | |
| $t_{pd}$ | CLK | Any Q | 2V | | 115 | 175 | | | 220 | |
| | | | 4.5V | | 23 | 35 | | | 44 | |
| | | | 6V | | 20 | 30 | | | 38 | |
| $t_t$ | | | 2V | | 38 | 75 | | | 95 | ns |
| | | | 4.5V | | 8 | 15 | | | 19 | |
| | | | 6V | | 6 | 13 | | | 16 | |

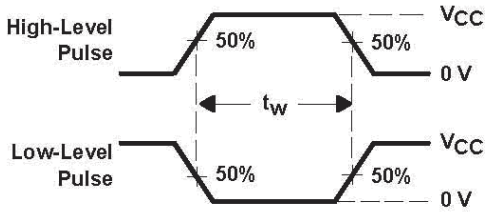
**Operating characteristics, $T_A$ = 25℃**

| PARAMETER | TESTCONDITIONS | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ Power dissipation capacitance | No load | 135 | pF |

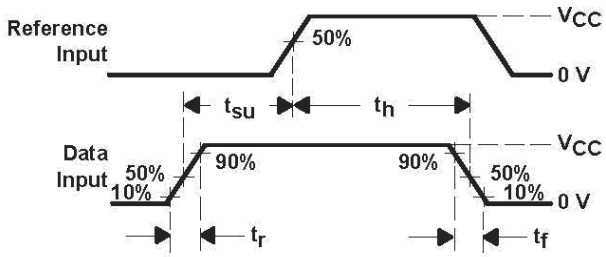
## PARAMETER MEASUREMENT INFORMATION



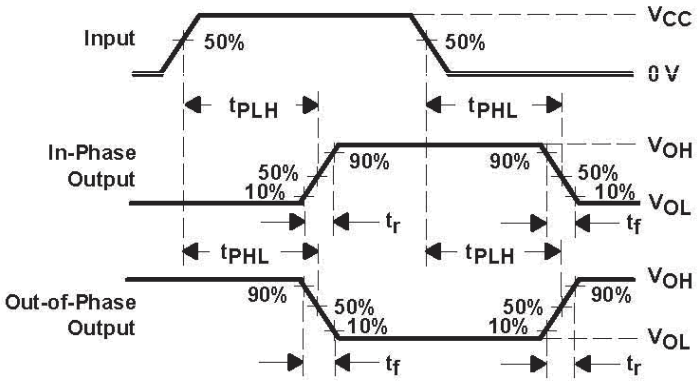

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

**NOTES:** A. $C_L$ includes probe and test-fixture capacitance.

B. Phase relation ships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR≤1MHz, $Z_O$ =50Ω, $t_r$ = 6ns, $t_f$ =6ns.

C. For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

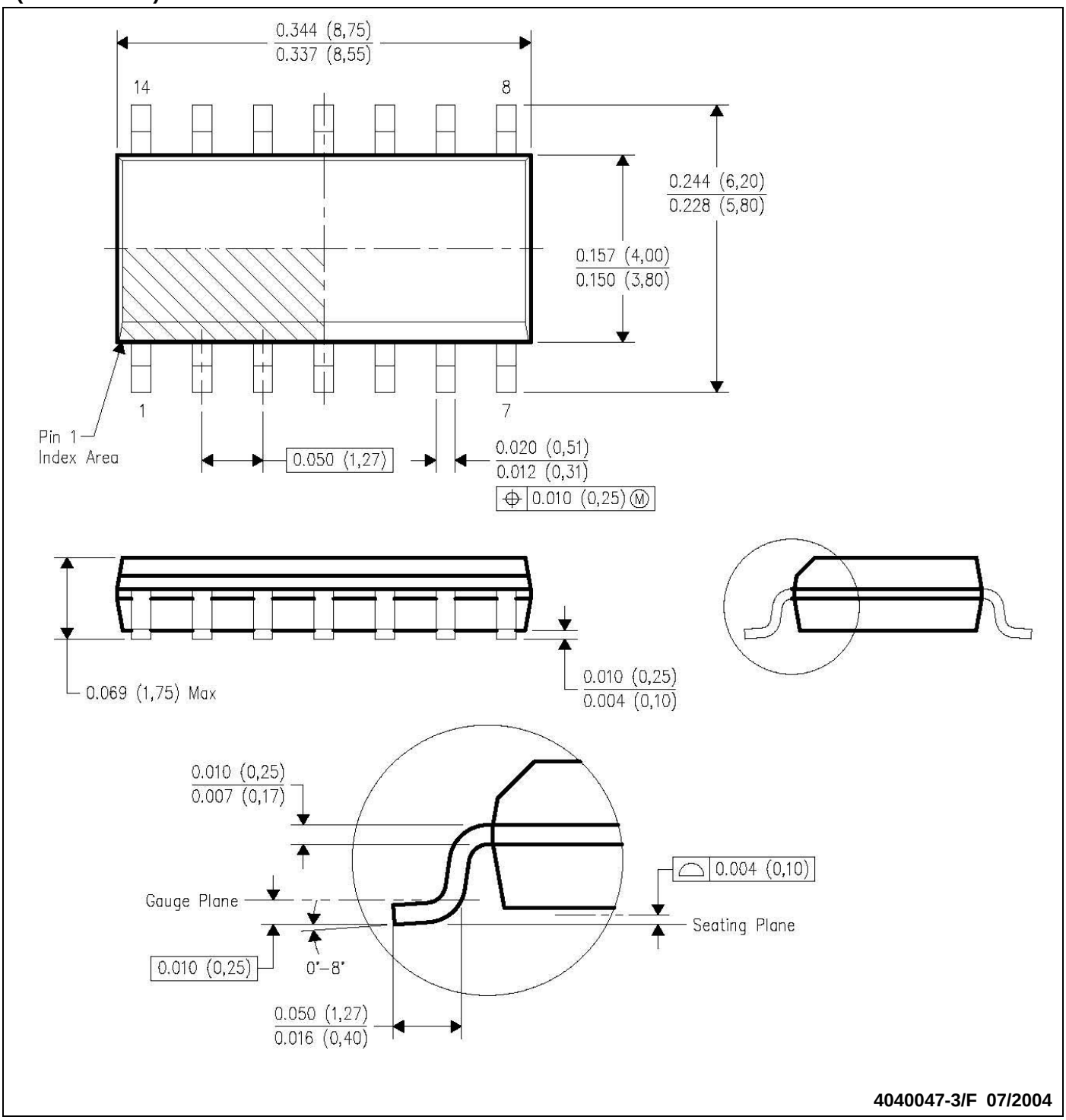
D. The outputs are measured one at a time with one input transition per measurement.

E. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

## MECHANICAL DATA

**D (R-PDSO-G14)** **PLASTIC SMALL-OUTLINE PACKAGE**




**NOTES:** A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).

D. Falls within JEDEC MS-012 variation AB.